

CLAIMS:

What is claimed is:

1. A high speed static multiplexer comprising:
 - a plurality of data inputs and at least one select input;
 - an output;
 - a high voltage rail and a low voltage rail;
 - a pull-up circuit coupled between said output and said high voltage rail and further coupled to said plurality of data inputs and said at least one select input, wherein said pull-up circuit generates a first logic state at said output in response to a selected data input having said first logic state; and
 - a pull-down circuit coupled between said output and said low voltage rail and further coupled to receive said plurality of data inputs and said at least one select input, wherein said pull-down circuit generates a second logic state at said output in response to a selected data input having said second logic state.
2. The high speed static multiplexer of Claim 1, wherein said pull-up circuit comprises:
 - a P-type transistor having a control node, and a first and second data node, coupled at said first data node to said output and at said second data node to said high voltage rail, wherein said P-type transistor exhibits signal swings less than said high voltage rail;
 - a plurality of N-type transistors, each having a control node, and a first and second data node, wherein said second data node of each of said plurality of N-type transistors is coupled to a control node of said P-type transistor, said first data node of each of said

13
14
15
16

1
2

3
4
5
6
7
8
9
0
1

1
2
3

1 5. A high-speed static multiplexer comprising:
2 at least two data inputs circuits that each receive
3 a respective data input;
4 at least one select input, wherein each of said at
5 least one select input receives a respective select
6 signal;
7 an output; and
8 a plurality of transistors operationally coupled
9 between said at least two data input circuits and said
10 output, wherein said plurality of transistors each have a
11 control node and a first and second data node and wherein
12 said plurality of transistors are controlled by both data
13 inputs and select signals to select of one of said data
14 inputs to yield said output.

1 6. The high speed static multiplexer of Claim 5,
2 wherein said plurality of transistors include a P-type
3 transistor and a plurality of sets of first, second, and
4 third N-type transistors for each of said at least two
5 data inputs.

1 7. The high-speed static multiplexer of Claim 6,
2 wherein each of said at least two data input circuits
3 includes an in-line inverter for inverting said
4 respective data input to produce an inverted input.

1 8. The high speed static multiplexer of Claim 7,
2 wherein:
3 each of said at least two data input circuits is
4 coupled to a control node of said third N-type transistor
5 and to a first data node of said first N-type transistor;
6 and

7 said at least one select signal input is coupled to
8 a control node of said first N-type transistor and to a
9 control node of said second N-type transistor;

1 9. The high speed static multiplexer of Claim 8,
2 wherein further:

3 a second data node of said first N-type transistor
4 is connected to a control node of said P-type transistor;

5 a second data node of said P-type transistor is
6 connected to a power supply (V_{DD}); and

7 a first data node of said P-type transistor is
8 connected to said output.

1 10. The high speed static multiplexer of Claim 9,
2 wherein further:

3 a second data node of said third N-type transistor
4 is connected to ground;

5 a first data node of said third N-type transistor is
6 coupled to a second data node of said second N-type
7 transistor; and

8 a first data node of said second N-type transistor
9 is coupled to said first data node of said P-type
10 transistor at said output.

1 11. The high speed static multiplexer of claim 6,
2 wherein said P-type transistor has an on state and off
3 state and wherein a voltage differential at said control
4 node to change between said on and off states is less
5 than the voltage differential between a high voltage
6 applied at a second data node of said P-type transistor
7 and a low voltage applied at a second data node of said
 third N-type transistor.

12. The high speed static multiplexer of claim 6, wherein said plurality of transistors are field effect transistors (FETs).

1 13. A multi-level high-speed static multiplexer
2 comprising:

3 a plurality of connected levels of high speed static
4 multiplexers, wherein each of said high speed
5 multiplexers comprises:

6 a plurality of data inputs and at least one
7 select input;

8 an output;

9 a high voltage rail and a low voltage rail;

10 a pull-up circuit coupled between said output
11 and said high voltage rail and further coupled to
12 said plurality of data inputs and said at least one
13 select input, wherein said pull-up circuit generates
14 a first logic state at said output in response to a
15 selected data input having said first logic state;
16 and

17 a pull-down circuit coupled between said output
18 and said low voltage rail and further coupled to
19 said plurality of data inputs and said at least one
20 select input, wherein said pull-down circuit
21 generates a second logic state at said output in
22 response to a selected data input having said second
23 logic state; and

24 wherein each of said outputs at a first level
25 of said plurality of levels is coupled to one of said
26 plurality of data inputs of said high speed static
27 multiplexers at a next level of said plurality of levels,
28 wherein a multiplicative-input multiplexer is realized
29 having $N \times M$ possible outputs, where N is a number of data
30 inputs at said first level and M is the number of data
31 inputs at the next level.

1 14. The multi-level high speed static multiplexer of
2 Claim 13, wherein said plurality of levels includes more
3 than two levels with a final level having a single high
4 speed static multiplexer, and wherein each of said
5 outputs of a given level is fed into at least one input
6 at a next level until said final level.

1 15. The multi-level high speed static multiplexer
2 circuit of Claim 14, wherein each even number of levels
3 yields a corrected output and each odd number of level
4 yields an inverted output.

1 16. The multi-level high speed static multiplexer of
2 Claim 15, further comprising an inverter coupled to each
3 of said data inputs at said first level when said number
4 of levels is odd.

1 17. The multi-level high speed static multiplexer of
2 Claim 15, further comprising an inverter coupled to said
3 output at said final level when said number of levels is
4 odd.